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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,606	07/28/2003	Shigeo Tokumitsu	67161-070	4273

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McDermott, Will & Emery
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER

MAGEE, THOMAS J

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/627,606

Applicant(s)

TOKUMITSU ET AL.

Examiner

Thomas J. Magee

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. ____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>07282003</u> . | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Claim Rejections – 35 U.S.C. 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 4, and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Chien (US 6,639,324 B1).

3. Regarding Claim 1, Chien discloses a semiconductor device comprising:

a semiconductor chip (20) diced from a semiconductor substrate with a prescribed element (See Figure 4) and an electrode portion (at 201) formed on its main face, and without removing a conductive film from its dicing line region (wherein the conductive film remains as a part of structure in pad area).

a conductive wire (at 26) (Col. 3, lines 61 – 64) connected to said electrode portion, and an insulating sheet ("layer") (24) (dielectric) covering part of said conductive film along the periphery (lateral edges) of said semiconductor chip (Figure 4).

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4. Regarding Claim 2, Chien discloses that the insulating sheet (dielectric) (epoxy) covers the back face (221) (Col. 3, lines 9 – 12), with the insulating sheet covering the side face and part of the front face along the periphery of the semiconductor chip (Col. 3, lines 30 -35) (Figure 4).

5. Regarding Claim 4, Chien discloses that the insulating sheet (24) covers the front face and side face of the semiconductor chip (Figure 2).

6. Regarding Claim 5, Chien discloses that an opening is formed (21) (Figure 2) at the wire locations in the insulating sheet at a position extending to said electrode portion during encapsulation (Col. 3, lines 44 – 49), wherein said conductive wire (Col. 3, lines 61 – 63) is connected to said electrode through said opening (Col. 3, lines 63 – 64).

Claim Rejections – 35 U.S.C. 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 3, and 6 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chien, as applied to Claims 1, 2, 4, and 5, and further in view of Duesman et al. (US

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6,449,161 B2).

9. Regarding Claims 3, and 6 – 8, Chien does not explicitly disclose that the semiconductor chips are layered, but does disclose that multiple semiconductor chips can be bonded onto the single heat sink (Col. 5, lines 51 – 55). Duesman et al. disclose that a heat sink (heat absorbing section) (22) can be inserted between chips (30,32) of a stack to conduct heat away (Col. 2, lines 50 – 54) (Figure 8). It would have then been obvious to one of ordinary skill in the art at the time of the invention to use the front and backside mounting procedure of Duesman et al. to mount chips in Chien, producing a layered structure, and to use the encapsulation procedures of Chien to encase the chips, thereby resulting in efficient heat transfer and balance of thermal stresses.

Conclusions

10. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658**. The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732**. The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306**.

Thomas Magee
September 7, 2004



EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800